

10-31-00

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PATENT

Attorney Docket No. SAM-151

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Won-Suk Yang, Sang-Ho Song, Hong-Sik Jeong, Ki-Nam Kim
 Filing Date: Herewith
 Title: Bit Line Landing Pad and Borderless Contact on Bit Line Stud With
 Localized Etch Stop Layer Formed in Void Region, and Manufacturing
 Method Thereof

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.10

"Express Mail" Mailing Label Number EL596759607US I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated below and is addressed to BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, DC 20231.

10/30/00
 Date

Anthony M. Flick
 Anthony M. Flick

BOX PATENT APPLICATION

Assistant Commissioner for Patents
 Washington, DC 20231

TRANSMITTAL LETTER

Sir:

Enclosed herewith for filing in the above-identified patent application please find the following listed items:

1. New Application Transmittal;
2. New Patent Application;
3. Executed Declaration, Petition and Power of Attorney;
4. Five (5) Sheets of Informal Drawings;
5. Check in the amount of \$710.00 to cover requisite fee;
6. Assignment Recordation Form Cover Sheet - - PTO-1595;
7. Executed Assignment;
8. Check in the amount of \$40.00 to cover assignment recordation fee;
9. Information Disclosure Statement;
10. Information Disclosure Form---PTO-1449;
11. Copies of Cited References; and
12. Return Postcard.

In connection with the foregoing matter, please charge any additional fees which may be due, or credit any overpayment, to Deposit Account Number 19-0079. A duplicate copy of this letter is provided for this purpose.

Respectfully submitted,

Date: October 30, 2000
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09699589-1030000

BOX PATENT APPLICATION
Assistant Commissioner for Patents
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Transmitted herewith for filing is the patent application of

For (title): BIT LINE LANDING PAD AND BORDERLESS CONTACT ON BIT LINE STUD WITH LOCALIZED ETCH STOP LAYER FORMED IN VOID REGION, AND MANUFACTURING METHOD THEREOF

Amy M. Flick
Print Name

4. Additional papers enclosed

- ☐ Preliminary Amendment
- ☒ Information Disclosure Statement (37 C.F.R. 1.98)
- ☒ Form PTO-1449 (PTO/SB/08A and 08B)
- ☒ Copies of cited references
- ☐ Declaration of Biological Deposit
- ☐ Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.
- ☐ Authorization of Attorney(s) to Accept and Follow Instructions from Representative
- ☐ Special Comments
- ☒ Other: Return Postcard.

5. Declaration or oath

- ☒ Enclosed
 - ☐ Unexecuted
 - ☒ Executed by
 - ☒ inventors
 - ☐ legal representative of inventor(s).
37 CFR 1.42 or 1.43.
 - ☐ joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached.
 - ☐ This is the petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 is also attached. See item 12 below for fee.
- ☐ Not Enclosed
- ☐ Application is made by a person authorized under 37 C.F.R. 1.41 (c) on behalf of all the above named inventor(s).
 - ☐ Showing that the filing is authorized.

6. Assignment

- ☒ An assignment of the invention to Samsung Electronics Co., Ltd.
 - ☒ is attached. A separate ☐ "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or ☒ FORM PTO 1595 is also attached. will follow.

7. Certified Copy

Certified copy(ies) of application(s)

Country	Appln. no.	Filed
Country	Appln. no.	Filed
Country	Appln. no.	Filed

from which priority is claimed

- ☐ is (are) attached.
☐ will follow.

8. Fee Calculation (37 C.F.R. 1.16)

CLAIMS AS FILED				
	Number filed		Number Extra	Rate
				Basic Fee 37 C.F.R. 1.16(a) \$710.00
Total Claims (37 CFR 1.16(c))	17	- 20 =	0	\$ 18.00
Independent Claims (37 CFR 1.16(b))	2	- 3 =	0	\$ 80.00
Multiple dependent claim(s), if any (37 CFR 1.16(d))			+	\$260.00

- ☐ A Preliminary Amendment canceling claims is enclosed. The filing fee is calculated based on the number of claims remaining after entry of the Preliminary Amendment.
☐ Amendment deleting multiple-dependencies is enclosed.
☐ Fee for extra claims is not being paid at this time.

Filing Fee Calculation

\$ 710.00

9. Small Entity Statement(s)

☐ Verified Statement(s) that this is a filing by a small entity under 37 CFR 1.9 and 1.27 is (are) attached.

☐ Status as a small entity was claimed in prior application _____, filed on _____
from which benefit is being claimed for this application under:

35 U.S.C. ☐ 119(e),

☐ 120,

☐ 121,

☐ 365(c),

and which status as a small entity is still proper and desired.

☐ A copy of the verified statement in the prior application is included.

Filing Fee Calculation (50% of A, B or C above)

\$ _____

10. Fee Payment Being Made at This Time

☐ Not Enclosed

☐ No filing fee is to be paid at this time.
(This and the surcharge required by 37 C.F.R. 1.16(e) can be paid subsequently.)

☒ Enclosed

☒ Basic filing fee \$ 710.00

☒ Recording assignment
(\$40.00; 37 C.F.R. 1.21(h))
(See attached "COVER SHEET FOR ASSIGNMENT
ACCOMPANYING NEW APPLICATION".) \$ 40.00

Total fees enclosed \$ 750.00

11. Method of Payment of Fees

☒ Checks in the amounts of \$ 710.00, 40.00

☐ Charge Account No. 19-0079 in the amount of \$ _____
A duplicate of this transmittal is attached.

12. **Authorization to Charge Additional Fees**

☒ The Commissioner is hereby authorized to charge the following additional fees during the entire pendency of this application to Account No. 19-0079.

☒ 37 C.F.R. 1.16(a), (f) or (g) (filing fees)

☒ 37 C.F.R. 1.16(b), (c) and (d) (presentation of extra claims)

☐ 37 C.F.R. 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)

☐ 37 C.F.R. 1.17 (application processing fees)

☐ 37 C.F.R. 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. 1.311(b))

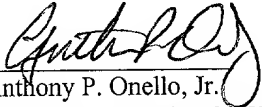
13. **Instructions as to Overpayment**

☒ Credit Account No. 19-0079

☐ Refund

Respectfully submitted,

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**BIT LINE LANDING PAD AND BORDERLESS CONTACT
ON BIT LINE STUD WITH LOCALIZED ETCH STOP LAYER FORMED IN VOID
REGION, AND MANUFACTURING METHOD THEREOF**

RELATED APPLICATIONS

The present application is related to United States Serial No. _____, entitled "Bit Line Landing Pad and Borderless Contact on Bit Line Stud with Etch Stop Layer and Manufacturing Method Thereof, filed of even date herewith; and United States Serial No. _____, entitled "Bit Line Landing Pad and Borderless Contact on Bit Line Stud with Localized Etch Stop Layer and Manufacturing Method Thereof", filed of even date herewith and incorporated herein by reference.

BACKGROUND OF THE INVENTION

In order to make more efficient use of integrated circuit surface area, conventional two-dimensional semiconductor technology has evolved such that contemporary circuits are formed on multiple layers in a three-dimensional configuration. In such configurations, active devices and interconnects are formed in a layered relationship. During the formation of each subsequent layer, an inter-layer pathway, referred to in the art as a "plug", or "stud" is electrically coupled between the various active devices and transmission lines of the different layers. To assist in aligning a plug, "landing pads" or "taps" are formed in lower layers to serve as a target for the plugs passing from the upper layer. The landing pads are coupled to an underlying circuit or interconnect and are generally larger in surface area than the circuit or interconnect to serve as a wider-tolerance target for the plug.

Such multi-layered technology has enabled the design of highly-integrated memory devices, for example DRAM devices, having extremely high capacity, for example above 1 gigabyte. Such DRAM devices include multiple arrays of memory cells, densely and efficiently laid out under tight design constraints. Between the cell areas are peripheral regions, which include supporting circuitry and interconnect circuitry between the cells, as well as input/peripherals, and the like.

Any misalignment between the vertical plugs and the horizontal interconnect features can cause defects and reliability problems. To ensure that the plug aligns with a feature, the features are made larger than required, for example through the use of landing pads. The area by which the feature is made larger is referred to in the art as a "border" around the vertical contact hole. Any excessive border area thus has a negative impact on circuit density.

5 Attempts have been made in the past to provide multiple layer interconnect, while reducing or eliminating the border area. These include circuits and fabrication procedures disclosed in United States Patent Nos. 6,083,824, 5,612,254, and 4,966,870.

10 To a larger extent, the packing density of circuits is limited by how closely the interconnect metal between circuits can be formed without encroaching on each other. These limits are dictated by design rules that govern the separation of one level of contact from another, and by design rules for nesting tolerance or for borders used around contacts.

15 Other efforts have made toward reducing the high-aspect ratio of the holes made for inter-level interconnects, where the aspect ratio refers the height of a hole as compared to its width. In general, the deeper the hole, the more difficult it is to fabricate the hole. Using the line of an underlying circuit, for example a bit line of a DRAM memory device, as a landing pad, the aspect ratio of the interconnection hole can be significantly reduced.

20 A typical multiple-layer DRAM memory device includes a cell region and a peripheral region. The cell region includes active switching devices, coupled to vertically-oriented capacitors, that serve as data storage devices. A cell bit line serves as an interconnect to transfer data between peripheral circuit regions and the cell region. The peripheral region includes a number of bit lines, that function as local interconnects, or studs, electrically coupling between the various active devices and transmission lines of the different layers. An insulative oxide layer is formed above the bit lines, and an interconnect stud is opened through the oxide layer and connected to the bit line.

25 When the bit lines are used for local interconnection, for example especially in sense amplifier regions, the layers of circuits can become very dense and crowded. For example, to access the bit line from an upper layer, the region between the bit lines must be accurately etched

to form a stud interconnect hole; both in a lateral direction, so as to avoid contact with adjacent bit lines, and in a vertical direction, so as to ensure that the hole is formed at the proper depth. Because the peripheral region, for example a sense amplifier region of a DRAM device, is often times densely populated with various interconnect paths, the cross-sectional area of any vertical stud interconnects should be minimized. Therefore, the above case requires subsequent formation of high-aspect-ratio studs that are difficult to achieve using contemporary fabrication processes.

Contemporary techniques of forming the interconnect stud are subject to several process limitations. These include horizontal misalignment, in a lateral direction, where the stud hole may be laterally misaligned with the underlying bit line during formation of the stud hole. Vertical misalignment can also occur, wherein the stud hole is not etched deep enough, so the stud does not make contact with the underlying bit line, or wherein the stud hole is etched too deeply, and is etched through the bit line.

To improve alignment accuracy, United States Patent No. 5,895,239 discloses a technique for employing a bit line landing pad together with a bit line stud. However, this approach requires tight tolerances at either, or both, the top portions of the bit lines, including the landing pad, and bottom portions of the upper interconnect stud, so as to provide a minimal width at the top of the bit line, and a maximum width at the bottom of the upper interconnect stud. A wide stud top limits circuit density considerations, while a narrow stud bottom leads to increased contact resistance and an increased aspect ratio that is difficult to accurately fabricate. No provision is made for vertical alignment of the stud, so if the stud hole is slightly misaligned with the underlying bit line, a void can be formed in the underlying inter-layer dielectric adjacent the stud.

Another approach at multiple-layered interconnect is disclosed in United States Patent No. 5,891,799. With reference to FIG. 1, in this approach, an etch-stop layer 206, for example a silicon nitride masking layer (Si_3N_4) is formed over an inter-layer dielectric (SiO_2) 202, in turn formed over a metal layer 210 formed on a substrate 200. Stud holes 213A, 213B are patterned through the mask layer 206 and underlying dielectric layer 202 for the deposit of studs 212A, 212B to connect between the upper and lower layers. Once the studs 212A, 212B are formed, the masking layer 206 later serves as an etching reference for studs 214A, 214B formed through

an upper masking layer 208 and upper dielectric layer 204. However, this technique suffers from a number of limitations. Since the Si_3N_4 masking layer 206, 208 is a high-stress-bearing material, and is formed indiscriminately as a layer over the entire circuit, this configuration imparts undue stress on the various layers, which may lead to warping of the circuit. Additionally, due to its high density, the masking layer prevents outgassing of impurities contained in the inter-layer dielectric, for example C, F, and Cl, during later high-temperature processes. The remaining Si_3N_4 masking layer would prevent the introduction of H_2 and O_2 during popular alloy processes, greatly affecting the conductive adhesiveness between the upper and lower metals.

Furthermore, this process is incompatible with contemporary memory fabrication processes, because the Si_3N_4 masking layer would be applied between bit lines. Dielectric spacers formed on each lateral side of a cell bit line prevent shorting between the cell bit line and the nearby capacitor. In order to make such spacers, it would be necessary to remove any masking layer between adjacent bit lines to allow for space for the capacitors to be inserted between the bit lines. However, this process would also remove any dielectric layer formed over the bit lines necessary for insulating the bit lines from the capacitors. This would also remove any masking layer on either side of the peripheral region bit lines, defeating the purpose of forming the masking layer in the first place.

SUMMARY OF THE INVENTION

The present invention is directed to a fabrication process and circuit that address the limitations of conventional techniques. For example, the present invention provides an etch-stop layer that is selectively patterned on only a portion of the underlying inter-layer dielectric, thereby allowing for outgassing during later fabrication processes. The remaining etch-stop layer is localized to only those portions surrounding the connecting media, for example surrounding the studs, between lower and upper contact holes. The surface area of the remaining etch-stop layer is preferably large enough so as to provide a suitable alignment target during formation of an overlying stud formed in an upper layer, yet small enough so as not to allow for sufficient

outgassing, and so as to not interfere with neighboring contact holes, for example contact holes for nearby bit line landing pads.

In one aspect, the present invention is directed to a semiconductor device comprising a first dielectric layer formed on a substrate. A second dielectric layer is formed on the first dielectric layer. A stud is formed through the first and second dielectric layers, and a third dielectric layer is formed over a top of the stud. A first pad of first etch stop material is formed over the top surface of the stud and under the third dielectric layer.

The pad is preferably formed in a void region remaining after removal of a portion of the second dielectric layer. The third dielectric layer and the first etch stop material may comprise the same material.

The semiconductor device may further comprise a first circuit region formed in the first dielectric layer, the first circuit region including the stud; and a second circuit region formed in the first dielectric layer, the second circuit region including at least one conductive line and at least one spacer on a sidewall of the conductive line, the spacer being made of the same material as the first pad of the first etch stop material.

A second pad of a second etch stop material may be formed over the top surface of the stud and the first pad of the first etch stop material, the second pad of the second etch stop material being selectively patterned to cover only an area of the semiconductor device that includes the stud. The third dielectric layer, and the first and second etch stop materials may comprise the same material.

The semiconductor device may further include a first circuit region formed in the first dielectric layer, the first circuit region including the stud; and a second circuit region formed in the first dielectric layer, the second circuit region including at least one conductive line and at least one spacer on a sidewall of the conductive line, the spacer being made of the same material as the first pad of the first etch stop material, whereby the spacers and the first pad are formed simultaneously.

The third dielectric layer preferably has an etch selectivity with respect to the second dielectric layer, and may comprises etch stop material.

In another aspect, the present invention comprises a method of forming a semiconductor device. A first dielectric layer is formed on a substrate and a second dielectric layer is formed on the first dielectric layer. A stud is provided through the first and second dielectric layers, and a third dielectric layer is formed over the top of the stud and the second dielectric layer. A portion of the second dielectric layer is removed at the top of the stud, to create a void region in the second dielectric layer at the top of the stud and under the third dielectric layer. A first pad of a first etch stop material is provided in the void region.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the invention will be apparent from the more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

FIG. 1 is a cutaway side view of a conventional multiple-layered interconnect configuration, illustrating the use of a etch-stop layer.

FIG. 2 is a cutaway side view of a multiple-layered interconnect configuration utilizing a selectively-patterned etch-stop layer, in accordance with the present invention.

FIGs. 3A-3F are cutaway side views, the left and right columns being sectioned along orthogonal axes, illustrating use of an etch-stop pad formed in a void formed above a connecting stud for a multiple-layered memory device including cell and peripheral regions, in accordance with the present invention.

FIGs. 4A-4F are cutaway side views, the left and right columns being sectioned along orthogonal axes, illustrating use of an etch-stop pad formed in a void formed above a connecting stud for a multiple-layered memory device including cell and peripheral regions, in accordance with an alternative embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Throughout the detailed description, the principles of the present invention are illustrated in the context of a memory device having cell and peripheral regions. It will be apparent to those skilled in the art that the circuits and processes of the present invention disclosed herein are equally applicable to other multiple-layered circuit embodiments.

5 FIG. 2 is a cutaway side view of a multiple-layered circuit configuration, in accordance with the present invention. A conductive layer pattern 210 is formed on a substrate 200. A first inter-layer dielectric 202 is provided over the conductive layer pattern. A second dielectric layer 203 is formed over the first 202. Contact holes 219A, 219B are formed in the inter-layer dielectric 202, and inter-layer contact studs 220A, 220B are provided in the contact holes 219A, 219B. A conductive line 222 is formed over one of the studs 220B, for example to later serve as a landing pad for an upper-level stud 230B.

10 A first etch-stop material layer 224A is selectively patterned on the upper surface of the lower-level stud 220A, and on a portion of the inter-layer dielectric 202 surrounding the lower-level stud 220A. The first etch-stop material layer 224B is further patterned on the conductive line 222. A second etch-stop material layer is patterned over the resulting structure, and selectively removed so as to provide for lateral spacers 226 on the side walls of the conductive line 222. The first and second etch-stop material layers may comprise similar, or different, materials, for example Si_3N_4 , Ta_2O_5 or Al_2O_3 .

15 A second inter-layer dielectric 204 is formed over the resulting structure, and upper-level
20 contact holes 229A, 229B are formed to provide for upper-level contact studs 230A, 230B. During formation of the holes 229A, 229B, the etch stop layers 224A, 224B serve as an alignment target to prevent over-etching of the underlying first interlayer dielectric 202 in the region surrounding the stud 220A, and to prevent over-etching of the landing pad 222. Following formation of the upper-level studs 230A, 230B, metal traces 232A, 232B are provided on the
25 resulting structure to complete the circuit.

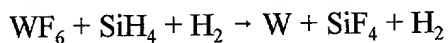
 An exemplary application of the configuration of the present invention will now be described with reference to FIGs. 3A-3F and FIGs. 4A-4F which illustrate sequential sectional

views of the formation of inter-level contacts in a memory device including cell and peripheral regions, in accordance with the present invention. The "X" and "Y" direction views represent sections taken along respective orthogonal axes of the device, for example along the bit line and word line directions, respectively.

In FIG. 3A, an active memory cell 240 is formed in a substrate 200 of a memory device. The memory device includes a cell region 242 comprising densely-packed memory cells 240 and data lines, and a peripheral region 244, including interconnect lines, and peripheral circuitry, for example input/output circuitry, that service the memory cell region 242. Collectively, in the context of a memory device application, the data lines and peripheral interconnect lines are referred to herein as "bit lines". However, as explained above, the present invention is equally applicable to other embodiments requiring layer-to-layer interconnect.

An first dielectric layer 202, for example high-density-plasma oxide is formed on the cell region 242 and the peripheral region 244 and substrate 200. A second dielectric layer 302, is formed above the first dielectric layer. The second dielectric layer 302 may comprise, for example, a relatively low-dielectric-constant material having, for example, a faster etch rate as compared to the first dielectric layer 202, such as BPSG, TOSZ, PE-Oxide, SOG, or FOX. A first etch stop layer 304, comprising, for example silicon nitride Si_3N_4 , is provided above the second dielectric layer.

Contact holes 219 are formed in the first etch stop layer 304 and first and second dielectric layers 202, 302, for example by etching, and contact studs 220A, 220B are provided in the holes 219, as shown in FIG. 3B. The contacts 220A, 220B are may be formed of tungsten, at a thickness of 500-2000 Angstroms. The gas reaction for deposition may comprise, for example:



at 40 Torr, and 415 C. Typical n+/p+ contact resistance values are in the range of 300-1000 ohms per contact, assuming a 0.15 μm - wide bit line to an n+ contact, and 1.5 - 5 kilohms per contact for a 0.23 μm bit line to a p+ contact.

Assuming a tungsten plug, the plug 220A, 220B may be formed by first providing a titanium Ti layer, for example by chemical vapor deposition (CVD) to a thickness of 100 Angstroms. This is followed by providing a layer of TiN, for example by chemical vapor deposition or atomic layer deposition (ALD) to a thickness of 300 Angstroms; followed by a layer of tungsten (W) of approximately 2000 Angstroms in thickness. The resulting structure is polished by chemical-mechanical polishing or etch-back processes.

Assuming a titanium nitride TiN plug, the plug 220A, 220B may be formed by first providing a titanium Ti layer, for example by chemical vapor deposition (CVD) to a thickness of 100 Angstroms. This is followed by providing a layer of TiN, for example by chemical vapor deposition to a thickness of 1500 Angstroms; followed by a chemical-mechanical polishing process.

In FIG. 3C, a bit line metal layer 252, for example tungsten, and a bit line capping layer 258, also referred to herein as a second etch stop layer, for example Si_3N_4 , are patterned over the studs 220B to be connected to bit lines. During patterning of the bit line material, a top portion of stud 220A is exposed, and therefore becomes partially etched to expose the second dielectric layer 302. Because the second dielectric layer 302 has a relatively fast etching rate, as compared to the first etch stop layer 304, a portion of the second dielectric layer 302 is removed below the first etch stop layer 304 through isotropic etching, undermining a circular ring under the first etch stop layer 304 about the upper surface of the stud 220A.

In FIG. 3D, a third etch-stop layer, for example comprising silicon nitride Si_3N_4 , is applied to the resulting structure and removed so as to form lateral spacers on the lateral sides of the bit lines, and also filling the undermined region 308A with third etch-stop material and providing lateral spacers 308B on the walls of the undermined region, above the stud 208A. For purposes of the present invention, the resulting third etch-stop material filling the undermined regions is referred to herein as a "pad". To accomplish this, the third etch-stop layer is provided to a thickness of 200-700 Angstroms, preferably less than 500 Angstroms, and is isotropically etched to form the bit line spacers 306 and stud hole spacers 308B. The third etch stop layer may comprise Si_3N_4 , Ta_2O_5 or Al_2O_3 , depending on the application. The resulting thickness of the third dielectric layer material 308A in the undermined region is preferably approximately twice the

lateral thickness of the sidewall spacers 306, 308B. For this reason, the thickness of the second inter-layer dielectric 302 is selected to match the resulting thickness of the dielectric layer.

In FIG. 3E, a third inter-layer dielectric layer 204 is formed over the resulting structure and storage node contact holes 262 are formed according to conventional techniques.

In FIG. 3F, the storage node contacts 264 are provided in the third inter-layer dielectric 204, and an fourth dielectric layer 266 is provided above the third 204. An upper-level contact hole 268 is provided in the dielectric layers 266, 204 using, for example, oxide etching, until the third etch-stop layer 308A, 308B becomes exposed. The third etch-stop layer 308A, 308B is used as a vertical guide for ensuring that the hole 268 properly exposes the top of the underlying stud 220A, without over-etching the underlying first inter-layer dielectric 202 at the sides of the underlying stud 220A in the stud coupling region. This is accomplished in a dual-step etching process that first etches through the third and fourth inter-layer dielectric layers 204, 266 comprising 1500W, 40mTorr, $C_4F_6 + O_2 + Ar$. Following this, etch-stop-layer attractive etching is performed using the underlying inter-layer dielectric 202 as an etch-stop to expose the top surface of the underlying stud 220A in a second etch process comprising 600 W, 50mTorr, $CHF_3 + Ar + H_2$, 105". For this reason, the third etch stop layer material 308A, 308B is preferably chosen to have different etching selectivity with respect to the underlying inter-layer dielectric 202.

In this manner, a connecting stud 220A is prepared for subsequent borderless contact formation. As a result, the circuit interconnection pattern can be accomplished in a relatively dense lateral configuration, for example in the dense configuration found in a peripheral region 244 of a semiconductor memory device.

To ensure proper vertical alignment and coupling of the lower and upper studs 270, 220A respectively, the third etch-stop layer 308A, 308B material is chosen so as to have a different etch selectivity as compared to that of the underlying first inter-layer dielectric insulating layer 202. In this manner, when forming upper stud hole 268, a first etch process can be used to accurately etch the third and second insulating dielectric layers 266, 204 to the upper surface of the first etch-stop layer 250. Following this, the first etch-stop material layer 250 is accurately etched in a second

etch process to the upper surface of the underlying stud 220A.

Similar procedures are applicable simultaneously, or separately with the above process for providing inter-layer studs (not shown in the drawings) for coupling to other bit-lines of the peripheral region, for example bit lines including bit-line landing pads 254.

An advantage of the FIG. 3 embodiment of the present invention lies in that the undermined opening occurs naturally, and therefore it is not necessary to photolithographically align the etch-stop regions relative to the studs.

FIGs. 4A-4F illustrate an alternative embodiment of the present invention. In FIGs. 4A, 4B, and 4C, inter-level studs 220A, 220B are formed through second and first inter-layer dielectric layers 202, 302 and a first etch-stop layer 304 as described above with reference to FIGs 3A - 3C. An undermined region of the second dielectric layer 320A is likewise formed below the first etch-stop layer 304, as described above.

In FIG. 4D, following application of the third etch-stop layer for forming the bit line spacers 306, before removal of the applied third etch-stop layer, a mask 322 is provided over the opening above stud 220A, in order to prevent removal of the third etch stop layer in that region 324. For this reason, the additional third etch stop layer material, both above 324A, and below 324B, remains, while any etch stop layer material 304 between the stud region and the bit line regions is removed.

Following this, the third and fourth dielectric layers, capacitors, and contacts are provided, as described above, and as shown in FIGs. 4E and 4F. As explained above, the remaining third etch-stop layer is used as an etch stop during etching of the upper-level stud holes 270. The hole etching process is similar to the process described above with reference to FIG. 3.

Due to the presence of the etch stop layer pad 308, 324 in the region above the stud 220A in the embodiments of FIGs. 3 and 4, overetching, profile degradation, and resultant bad step coverage are avoided in the present invention. Accordingly, contact-induced bit failures are likewise reduced.

Additionally, since the etch stop layer pad 308, 324 is localized to the region of the top of the stud 220A, outgassing during subsequent processes, as well as related alloying issues, are

While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

5 For example, in an alternative embodiment, rather than a single metal deposition step, separate photolithographic processes may be employed to provide the metal contacts on the bit line patterns and the metal contact on the bit line stud.

We claim:

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- 15
- 20
- 25

5

7 The semiconductor device of claim 1 further comprising:

a second circuit region formed in the first dielectric layer, the second circuit region including at least one conductive line and at least one spacer on a sidewall of the conductive line, the spacer being made of the same material as the first pad of the first etch stop material, whereby the spacers and the first pad are formed simultaneously.

20

9 The semiconductor device of claim 1 wherein the third dielectric layer comprises etch stop material.

- 10 A method of forming a semiconductor device comprising:
- forming a first dielectric layer on a substrate;
- forming a second dielectric layer on the first dielectric layer;
- forming a stud through the first and second dielectric layers;
- forming a third dielectric layer over the top of the stud and the second dielectric
- 5 layer;
- removing a portion of the second dielectric layer at the top of the stud, to create a
- void region in the second dielectric layer at the top of the stud and under the third
- dielectric layer; and
- forming a first pad of a first etch stop material in the void region.
- 11 The method of claim 10 further comprising:
- forming a first circuit region in the first dielectric layer, the first circuit region
- including the stud;
- forming a second circuit region in the first dielectric layer, the second circuit
- region including at least one conductive line.
- 12 The method of claim 11 further comprising forming a spacer of the first etch stop material
- on a sidewall of the conductive line while the pad of the first etch stop material is formed
- in the void region.
- 20 13 The method of claim 10 wherein the third dielectric layer and the first etch stop materials
- are the same material.
- 14 The method of claim 10 further comprising forming a second pad of a second etch stop
- 25 material over the top surface of the stud and the first pad of the first etch stop material.

15 The method of claim 14 wherein the third dielectric layer material and the first and second etch stop materials are the same material.

16 The method of claim 14 wherein forming the second pad of the second etch stop material comprises:

5 forming a layer of the second etch stop material on the device;
 selectively removing the layer of the second etch stop material to leave the second pad of the second etch stop material over the stud.

17 The method of claim 10 wherein the step of removing removes a top portion of the stud to further expose the second dielectric layer at the top of the stud.

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BIT LINE LANDING PAD AND BORDERLESS CONTACT
ON BIT LINE STUD WITH LOCALIZED ETCH STOP LAYER FORMED IN VOID
REGION, AND MANUFACTURING METHOD THEREOF

ABSTRACT OF THE DISCLOSURE

5 An etch-stop layer is selectively provided between layers of a multiple-layered circuit in a selective manner so as to allow for outgassing of impurities during subsequent fabrication processes. The etch-stop layer is formed over an underlying stud so as to serve as an alignment target during formation of an overlying stud formed in an upper layer. In this manner multiple-layered circuits, for example memory devices, can be fabricated in relatively dense configurations.

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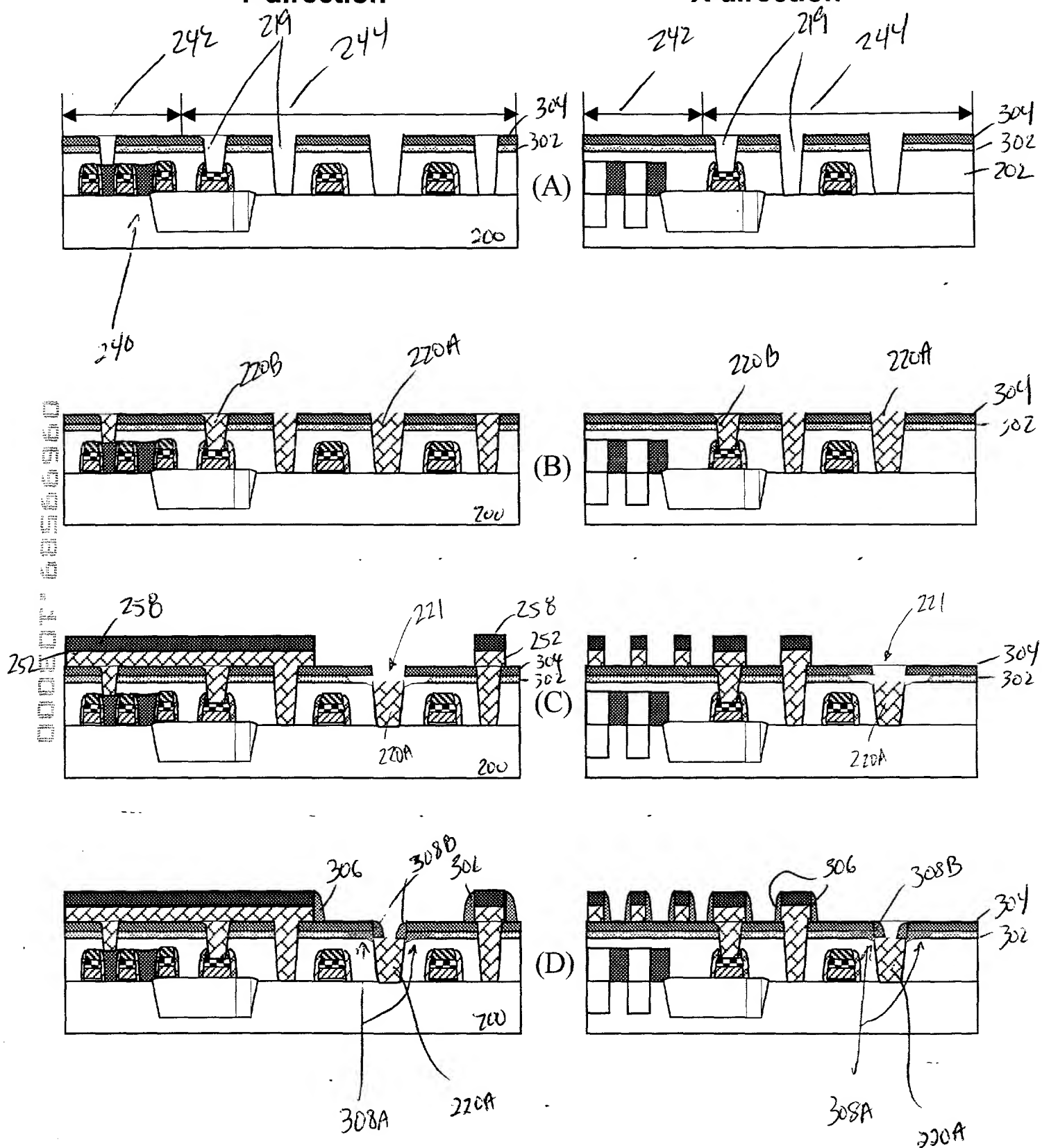
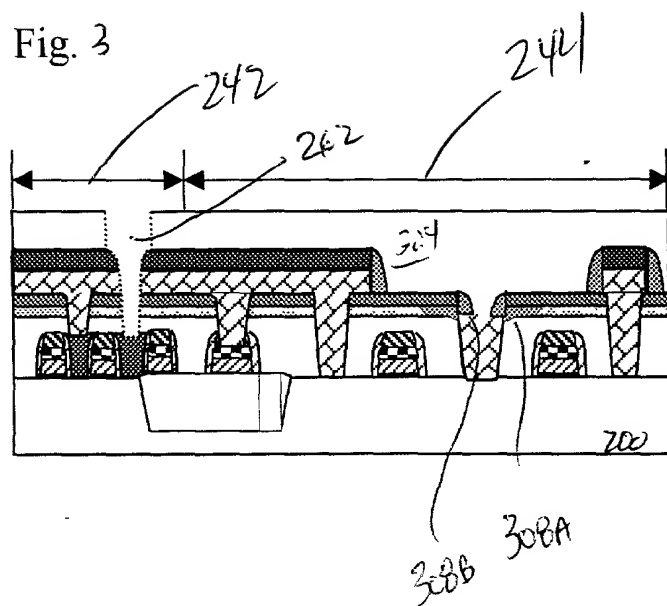
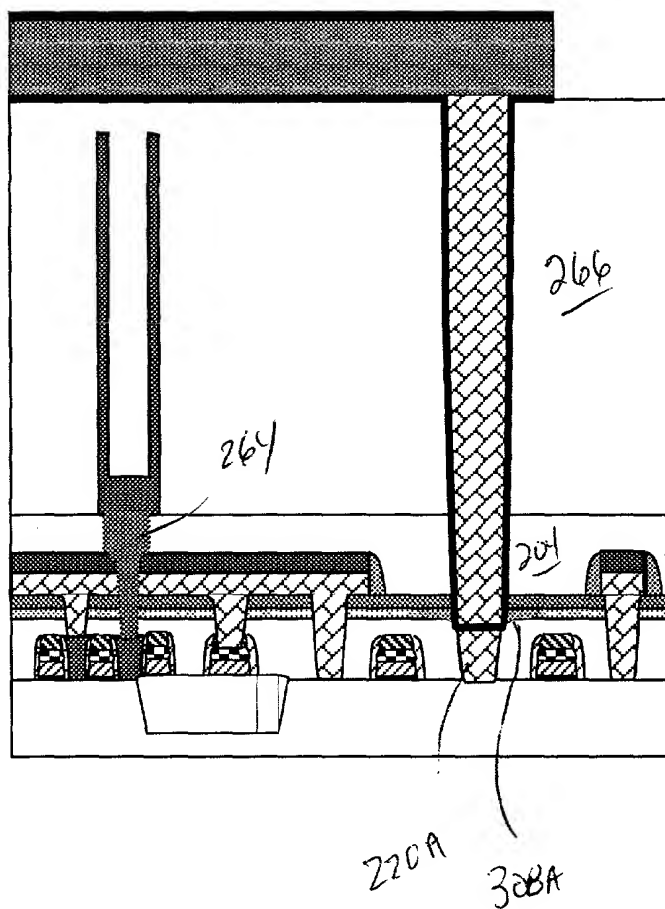
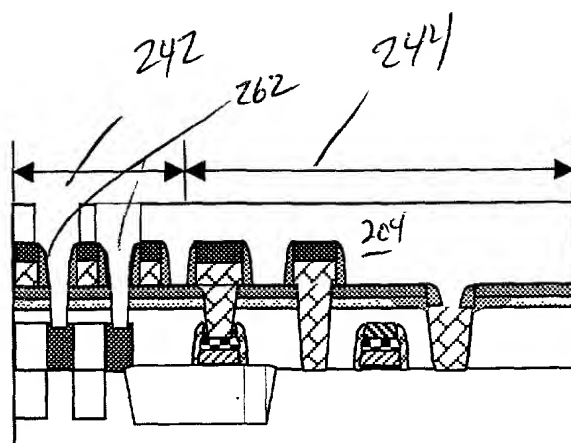


Fig. 3



(E)



(F)

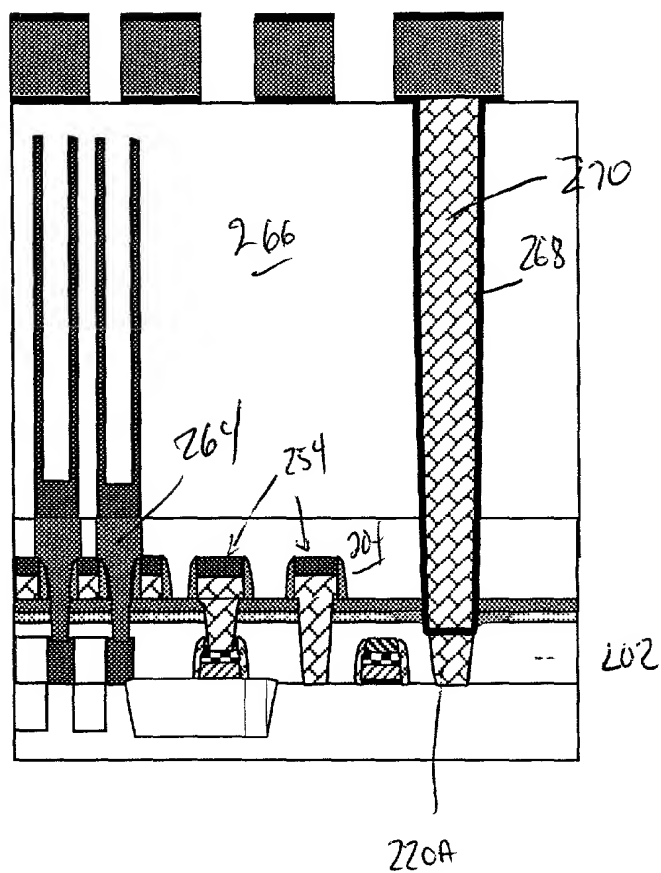
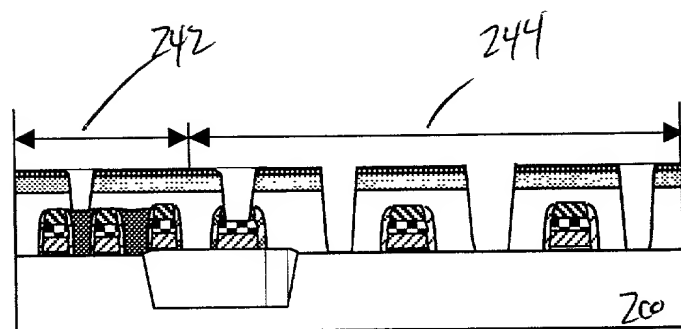


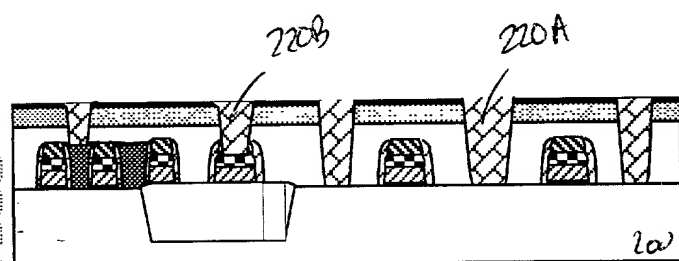
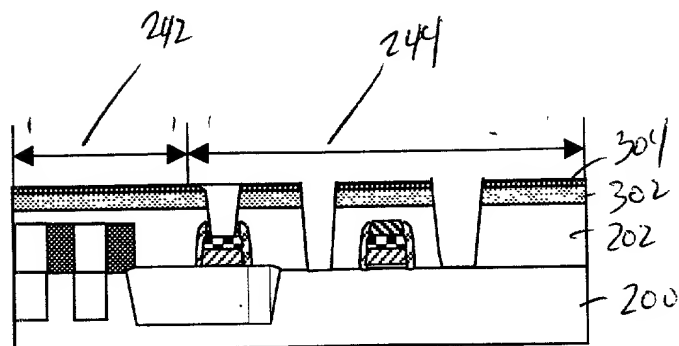
Fig. 4

Y direction

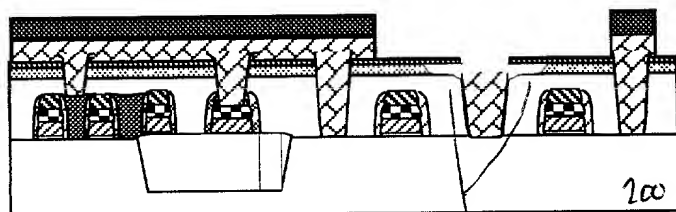
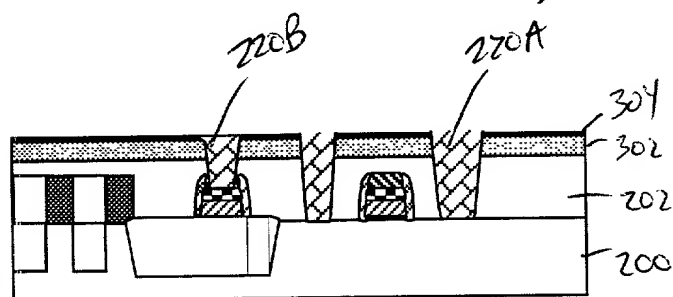
X direction



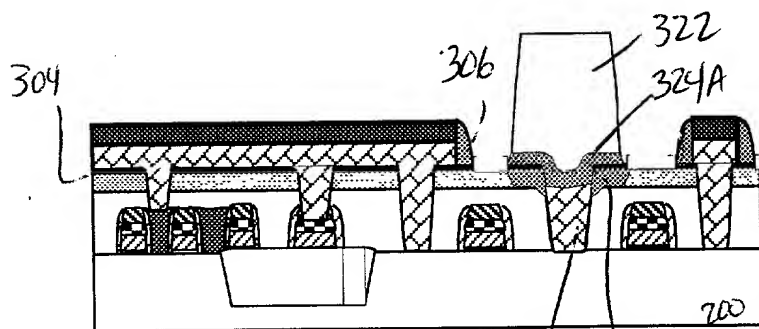
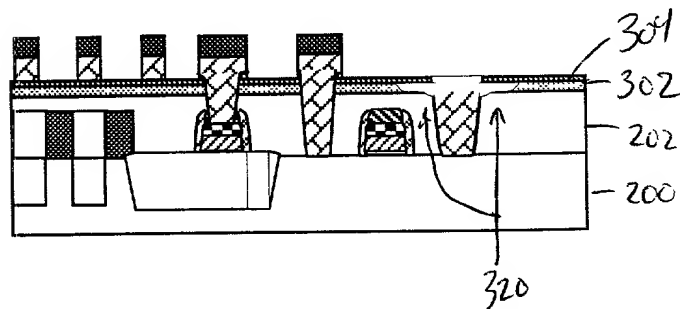
(A)



(B)



(C)



(D)

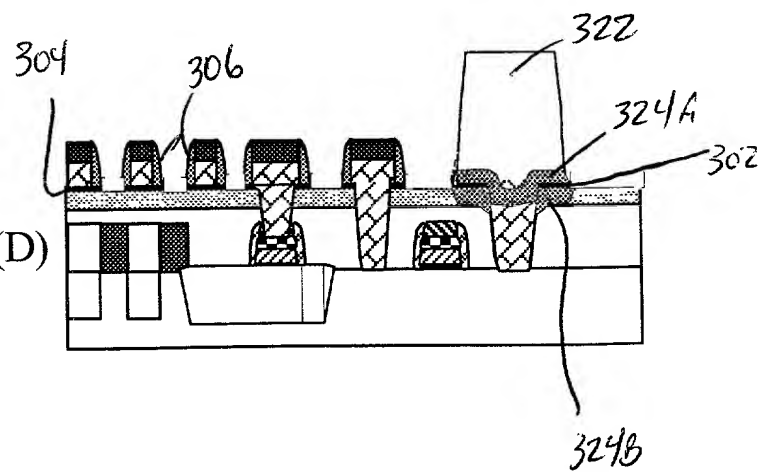
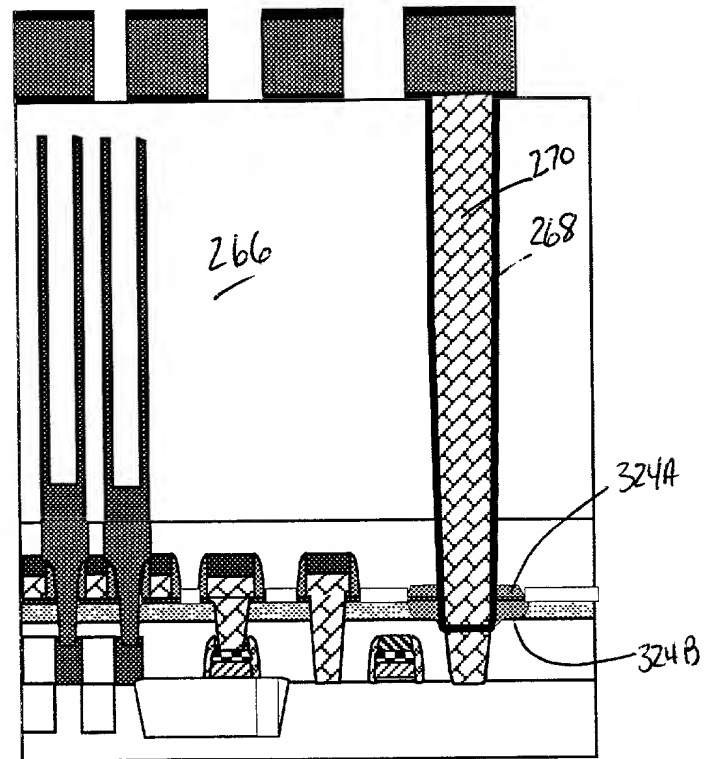
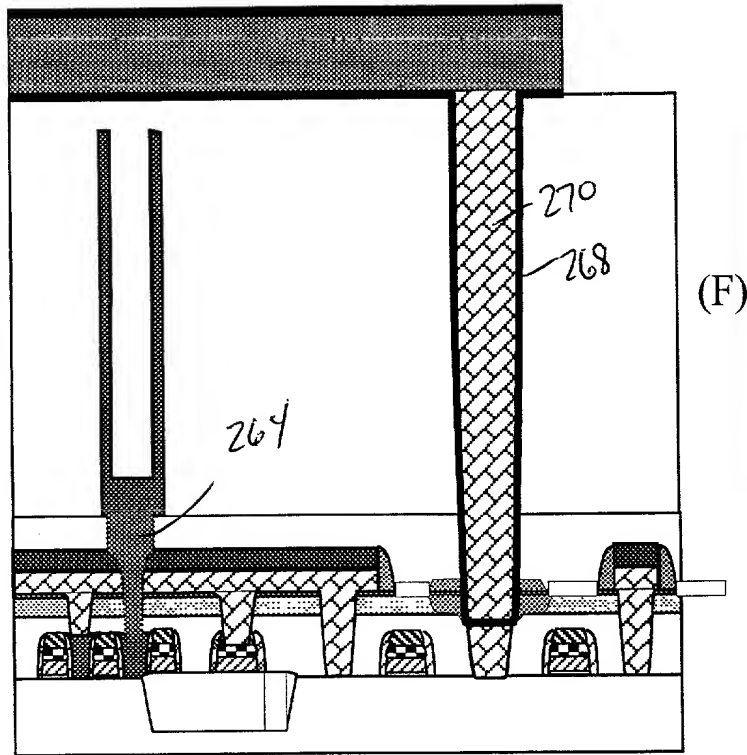
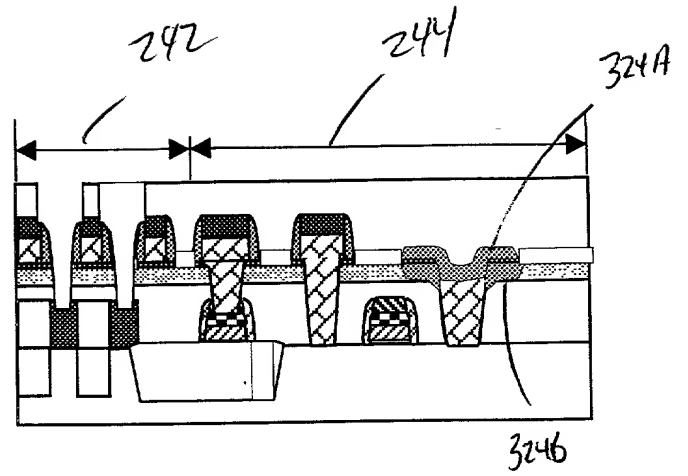
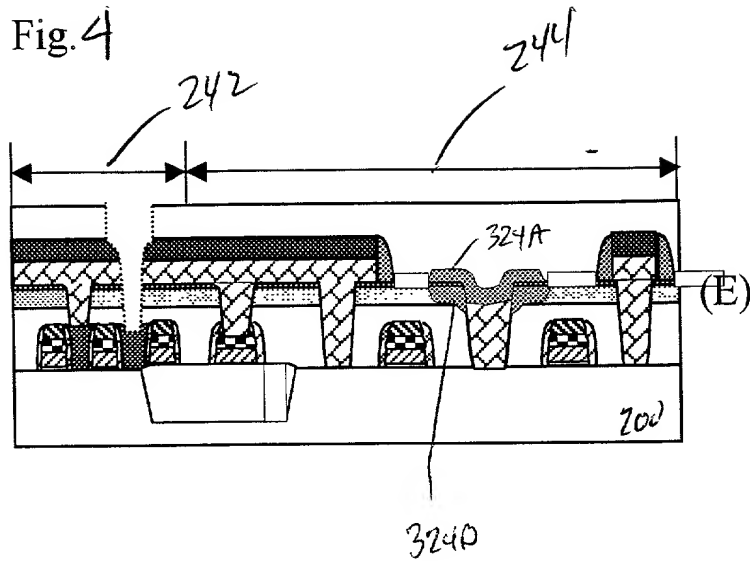


Fig. 4



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DECLARATION, PETITION AND POWER OF ATTORNEY FOR
PATENT APPLICATION

Attorney Docket No:

SAM-151—

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Bit Line Landing Pad and Borderless Contact on Bit Line Stud with Localized Etch-Stop Layer Formed in Void Region, and Manufacturing Method Thereof

the specification of which (check only one):

is attached hereto

were filed as United States Patent Applications

Судия №.

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and was amended

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(if applicable)

was filed as PCT Patent Application

Serial N.:

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and was amended under PCT Article 19

on .

(if applicable)

I hereby state that I have reviewed and understand the contents of the specification, including the claims as amended by any amendment referred to herein.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119:

COUNTRY (If PCT indicate PCT)	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. § 119 (YES/NO)

DECLARATION, PETITION AND POWER OF ATTORNEY FOR PATENT APPLICATION		Attorney Docket No: SAM-151	
I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.			
PRIOR U.S. APPLICATIONS FOR BENEFIT UNDER 35 U.S.C. § 119(e):			
APPLICATION NUMBER		FILING DATE	
I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:			
PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATION(S) DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. § 120:			
APPLICATION NUMBER (if PCT indicate PCT)		DATE OF FILING (day, month, year)	STATUS: (PATENTED, PENDING OR ABANDONED)
POWER OF ATTORNEY As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.			
Maurice E. Gauthier	Reg. No. 20,798	Patrick J. O'Shea	Reg. No. 35,305
Richard L. Stevens	Reg. No. 24,445	Arlene J. Powers	Reg. No. 35,985
Matthew E. Connor	Reg. No. 33,298	Steven M. Mills	Reg. No. 36,610
William E. Hilton	Reg. No. 33,192	Anthony P. Onello, Jr.	Reg. No. 38,572
Send Correspondence to		Direct Telephone Calls to:	
Steven M. Mills, Esq. Samuels, Gauthier & Stevens LLP 220 Franklin Street Boston, Massachusetts 02110		Steven M. Mills, Esq. (617) 426-9180 Ext. 149 (617) 426-2275 (facsimile)	
Wherefore I petition that letters patent be granted to me for the invention or discovery described and claimed in the attached specification and claims, and hereby subscribe my name to said specification and claims and to the foregoing declaration, power of attorney, and this petition.			
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that those statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.			
Signature <i>Won-Suk Kang</i>		Date <i>October 27, 2000</i>	
Full Name of 1st Inventor	Family Name Yang	First Given Name Won-Suk	Surname Given Name
Residence & Citizenship	City Yongin City, Kyungki-Do	State or Foreign Country Republic of Korea	Country of Citizenship Republic of Korea
Post Office Address	Post Office Address Poanglim APT 101-507, Dongchun-Ri, Sooji-Eup	City Yongin-City, Kyungki-Do	State & Foreign Country Republic of Korea

Attorney Docket No:
SAM-151 - -

Sang-Ho Song

October 16, 2000

Signature

Hong-sik Jeong

October 26, 2000

Signature

Ki-Nam Kim

October 26, 2000

Full Name of 4th Inventor	Family Name Kim	First Given Name KI-Nam	Second Given Name
Residence & Citizenship	City Anyang-City, Kyungki-Do	State or Foreign Country Republic of Korea	Country of Citizenship Republic of Korea
Post Office Address	Post Office Address Kummunal 1 Il APT 108-502, Pyungchon-Dong, Dongan-Ku	City Anyang-City, Kyungki-Do	State & Zip Code/Country Republic of Korea

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